Welldisk Technology Corp.

CompactFlash Memory Card

Datasheet

W03P03-XXXXX

1GB、2GB、4GB、8GB

Version 1.1

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Welldisk Technology Co,. Ltd.
layer 415 newmaterial chuangye building FengHui middle road no.7 Beijing haidian district
TEL: +86-010-56298618 E-mail: sales@welldisk.com

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Revision History

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Welldisk

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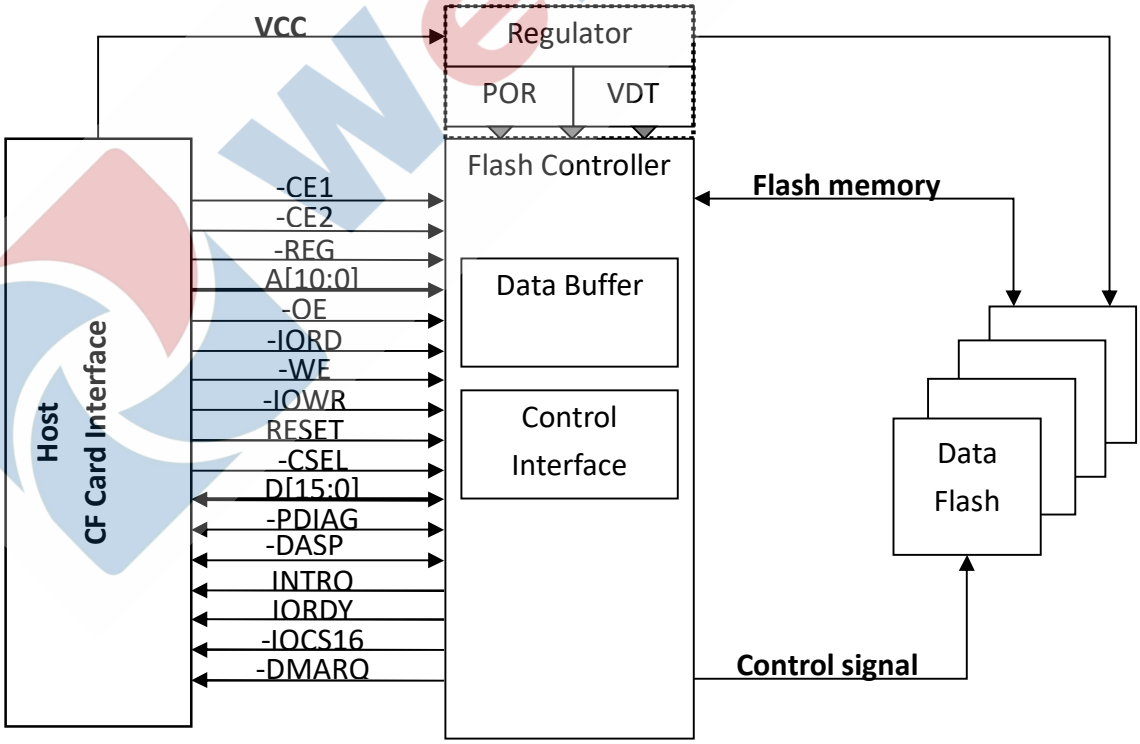
layer 415 newmaterial chuangye building FengHui middle road no.7 Beijing haidian district
TEL: +86-010-56298618 E-mail: sales@welldisk.com

1. INTRODUCTION

1.1. General Description

CompactFlash™ Cards are design base on CompactFlash™ Card Specification 4.1 compliant. It make up of a flash memory controller and NAND-Type flash memory. It can support a capacity of 1GB, 2GB, 4GB, 8GB. The CompactFlash™ card come with Standard operating temperature grad (0℃~+70 ℃) and Wide operating temperature grade (-40ºC ~+85ºC) to fulfill various specialized applications in normal or harsh operating environments. CompactFlash™ Card is ideal solutions for critical applications which request for long term supply with consistent key components.

1.2. Block Diagram



CF Card Block Diagram

2. FEATURES

- CompactFlash™ Card Specification 4.1 compliant
- Operating Modes:
  - PC Card Memory Mode.
  - PC Card I/O Mode.
  - True-IDE Mode.
- Ultra DMA Mode supported up to Mode 4
- Hardware RS-code ECC capable of correcting 24 bits in a 1,024-byte data
- Reliable wear-leveling algorithm to ensure the best of flash endurance.
- Very low power consumption
- Very high performance
- Rugged environment is working well
- Automatic error correction and retry capabilities
- Supports power down commands and Auto Stand-by / Sleep Mode
- +5 V ±10% or +3.3 V ±5% operation
- Low weight
- Noiseless
- MTBF > 2,000,000 hours
- Minimum 10,000 insertions
- Support S.M.A.R.T. Command
- Capacity: 1GB, 2GB, 4GB, 8GB

3. PRODUCT SPECIFICATIONS

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

3.1. System Environmental Specification

Referral Part Number		W03P03-XXXXX
Standard Temperature	Operating	0ºC ~ +70ºC
	Non-operating	-20ºC ~ +80ºC
Wide Temperature	Operating	-40ºC ~ +85ºC
	Non-operating	-50ºC ~ +95ºC
Humidity	Operating	5% ~ 95% non-condensing
	Non-operating	
Vibration	Operating	15G peak-to-peak maximum
	Non-operating	
Shock	Operating	2000 G maximum
	Non-operating	
Altitude	Operating	50,000 feet maximum
	Non-operating	

3.2. System Power Requirement

Referral Part Number		W03P03-XXXXX
DC Input Voltage 100mV max. ripple (p-p)		5V±10%
+5V Current (Maximum average value)	Standby Mode:	12.5 mA
	Reading Mode:	120 mA
	Writing Mode:	160mA

3.3. System Performance

Data Transfer Rate To/From Flash		25 Mbytes /sec burst
Data Transfer Rate To/From Host	**Ultra DMA mode 4**	66 Mbytes /sec burst
	PIO mode 4	16.6Mbytes /sec burst
1GB SLC	**Sequential Read**	30 M bytes / sec Max.
	Sequential Write	27 M bytes / sec Max.
2GB SLC	**Sequential Read**	30 M bytes / sec Max.
	Sequential Write	27 M bytes / sec Max.
4GB SLC	**Sequential Read**	53 M bytes / sec Max.
	Sequential Write	32 M bytes / sec Max.
8GB SLC	**Sequential Read**	53 M bytes / sec Max.
	Sequential Write	32 M bytes / sec Max.

3.4. System Reliability

MTBF	> 2,000,000 hours
Data Reliability	< 1 non-recoverable error in 10^{14} bits read < 1 erroneous correction in 10^{20} bits read
Wear-leveling Algorithms	Supportive
ECC Technology	Hardware RS-code ECC capable of correcting 24 bits in a 1,024-byte data
Endurance (SLC)	Greater than 60,000 cycles Logically contributed by Wear-leveling and advanced bad sector management
Data Retention	10 years

3.5. Capacity Specification

The specific capacities for the various models and the default number of heads, sectors and cylinders.

Capacity	Default Cylinder	Default Head	Default Sector	User Data Size
1GB	1,966	16	63	Depended on file management
2GB	3,900	16	63	
4GB	7,785	16	63	
8GB	15,538	16	63	

4. INTERTFACE DESCRIPTION

4.1. Pin Assignments

	Memory card mode		I/O card mode		True IDE mode	
Pin NO.	Signal name	I/O	Signal name	I/O	Signal name	I/O
1	GND	—	GND	—	GND	—
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	-CE1	I	-CE1	I	-CE0	I
8	A10	I	A10	I	A10[2]	I
9	-OE	I	-OE	I	-ATA SEL	I
10	A9	I	A9	I	A9[2]	I
11	A8	I	A8	I	A8[2]	I
12	A7	I	A7	I	A7[2]	I
13	VCC	—	VCC	—	VCC	—
14	A6	I	A6	I	A6[2]	I
15	A5	I	A5	I	A5[2]	I
16	A4	I	A4	I	A4[2]	I
17	A3	I	A3	I	A3[2]	I
18	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	-IOIS16	O	-IOCS16	O
25	-CD2	O	-CD2	O	-CD2	O
26	-CD1	O	-CD1	O	-CD1	O
27	D11[1]	I/O	D11[1]	I/O	D11[1]	I/O
28	D12[1]	I/O	D12[1]	I/O	D12[1]	I/O

29	D13[1]	I/O	D13[1]	I/O	D13[1]	I/O
	Memory card mode		**I/O card mode**		**True IDE mode**	
Pin NO.	**Signal name**	**I/O**	**Signal name**	**I/O**	**Signal name**	**I/O**
30	D14[1]	I/O	D14[1]	I/O	D14[1]	I/O
31	D15[1]	I/O	D15[1]	I/O	D15[1]	I/O
32	-CE2[1]	I	-CE2[1]	I	-CE1[1]	I
33	-VS1	O	-VS1	O	-VS1	O
34	-IORD	I	-IORD	I	-IORD[7] HSTROBE[8] -HDMARDY[9]	I
35	-IOWR	I	-IOWR	I	-IOWR[7] STOP[8, 9]	I
36	-WE	I	-WE	I	-WE[3]	I
37	RDY/-BSY	O	-IREQ	O	INTRQ	O
38	VCC	—	VCC	—	VCC	—
39	-CSEL[5]	I	-CSEL[5]	I	-CSEL	I
40	-VS2	O	-VS2	O	-VS2	O
41	RESET	I	RESET	I	-RESET	I
42	-WAIT		-WAIT	O	-IORDY[7] -DDMARDY[8] DSTROBE[9]	O
43	-INPACK	O	-INPACK	O	DMARQ	O
44	-REG	I	-REG	I	-DMACK[6]	I
45	BVD2	I/O	-SPKR	I/O	-DASP	I/O
46	BVD1	I/O	-STSCHG	I/O	-PDIAG	I/O
47	D8[1]	I/O	D8[1]	I/O	D8[1]	I/O
48	D9[1]	I/O	D9[1]	I/O	D9[1]	I/O
49	D10[1]	I/O	D10[1]	I/O	D10[1]	I/O
50	GND	—	GND	—	GND	—

Note:

1) These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.

2) The signal should be grounded by the host.

3) The signal should be tied to VCC by the host.

4) ***The mode is optional for CF+ Cards, but required for CompactFlash™ Storage Cards.***

5) ***The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.***

6) ***If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal, including a floating condition***

7) ***Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.***

8) ***Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.***

9) ***Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.***

4.2. Pin Descriptions

Signal Name	Dir.	Pin	Description
A10 – A00 (PC Card Memory Mode)	I	8,10,11,12, 14,15,16,17, 18,19,20	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card or CF+ Card, the memory mapped port address registers within the CompactFlash Storage Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers.
A10 – A00 (PC Card I/O Mode) A02 - A00 (True IDE Mode)	I	18,19,20	This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, only A [02:00] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded
BVD1 (PC Card Memory Mode) -STSCHG (PC Card I/O Mode) Status Changed -PDIAG (True IDE Mode)	I/O	46	This signal is asserted high, as BVD1 is not supported. This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register. In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.

BVD2 (PC Card Memory Mode) -SPKR (PC Card I/O Mode) -DASP (True IDE Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported. This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated. In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode) -CD1, -CD2 (PC Card I/O Mode) -CD1, -CD2 (True IDE Mode)	O	26,25	These Card Detect pins are connected to ground on the CompactFlash Storage Card or CF+ Card. They are used by the host to determine that the CompactFlash Storage Card or CF+ Card is fully inserted into its socket. This signal is the same for all modes. This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable -CE1, -CE2 (PC Card I/O Mode) Card Enable -CS0, -CS1 (True IDE Mode)	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Table 30, Table 33, Table 35, Table 39, Table 41 and Table 42. While (-) DMACK is asserted, -CE1 and -CE2 shall be held negated and the width of the transfers shall be 16 bits. This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode, -CS0 is the address range select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register.
-CSEL (PC Card Memory Mode) -CSEL (PC Card I/O Mode) -CSEL (True IDE Mode)	I	39	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.

D15 - D00 (PC Card Memory Mode) D15 - D00 (PC Card I/O Mode) D15 - D00 (True IDE Mode)	I/O	31,30,29,28, 27,49,48,47, 6,5,4,3,2, 23, 22, 21	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, all Task File operations occur in byte mode on the low order bus D [7:0] while all data transfers are 16 bit using D[15:0].
GND (PC Card Memory Mode) GND (PC Card I/O Mode) GND (True IDE Mode)	--	1,50	Ground. This signal is the same for all modes. This signal is the same for all modes.
-IORD (PC Card Memory Mode except Ultra DMA Protocol Active) -IORD (PC Card I/O Mode except Ultra DMA Protocol Active) -IORD (True IDE Mode – Except Ultra DMA Protocol Active) -HDMARDY (All Modes - Ultra DMA Protocol DMA Read) HSTROBE (All Modes - Ultra DMA Protocol DMA Write)	I	34	This signal is not used in this mode. This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card or CF+ Card when the card is configured to use the I/O interface. In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode. In all modes when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate – HDMARDY to pause an Ultra DMA transfer. In all modes when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.

-IOWR (PC Card Memory Mode – Except Ultra DMA Protocol Active) -IOWR (PC Card I/O Mode – Except Ultra DMA Protocol Active) -IOWR (True IDE Mode – Except Ultra DMA Protocol Active) STOP (All Modes – Ultra DMA Protocol Active)	I	35	This signal is not used in this mode. The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card or CF+ Card controller registers when the CompactFlash Storage Card or CF+ Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge). In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol. In All Modes, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA data burst.
-OE (PC Card Memory Mode) -OE (PC Card I/O Mode) -ATA SEL (True IDE Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers. In PC Card I/O Mode, this signal is used to read the CIS and configuration registers. To enable True IDE Mode this input should be grounded by the host.
READY (PC Card Memory Mode) -IREQ (PC Card I/O Mode) INTRQ (True IDE Mode)	O	37	In Memory Mode, this signal is set high when the CompactFlash Storage Card or CF+ Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF+ Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state. I/O Operation – After the CompactFlash Storage Card or CF+ Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode

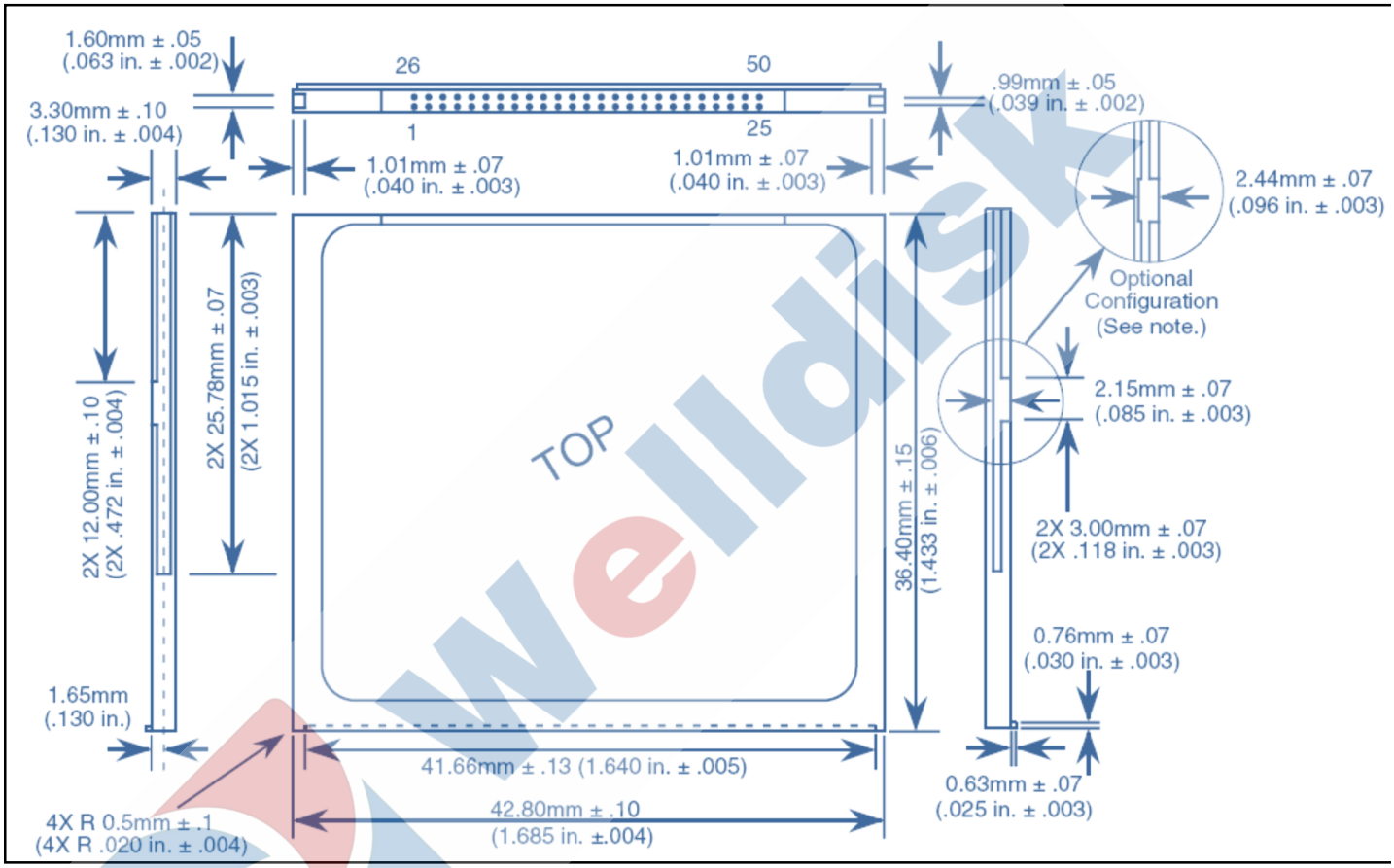
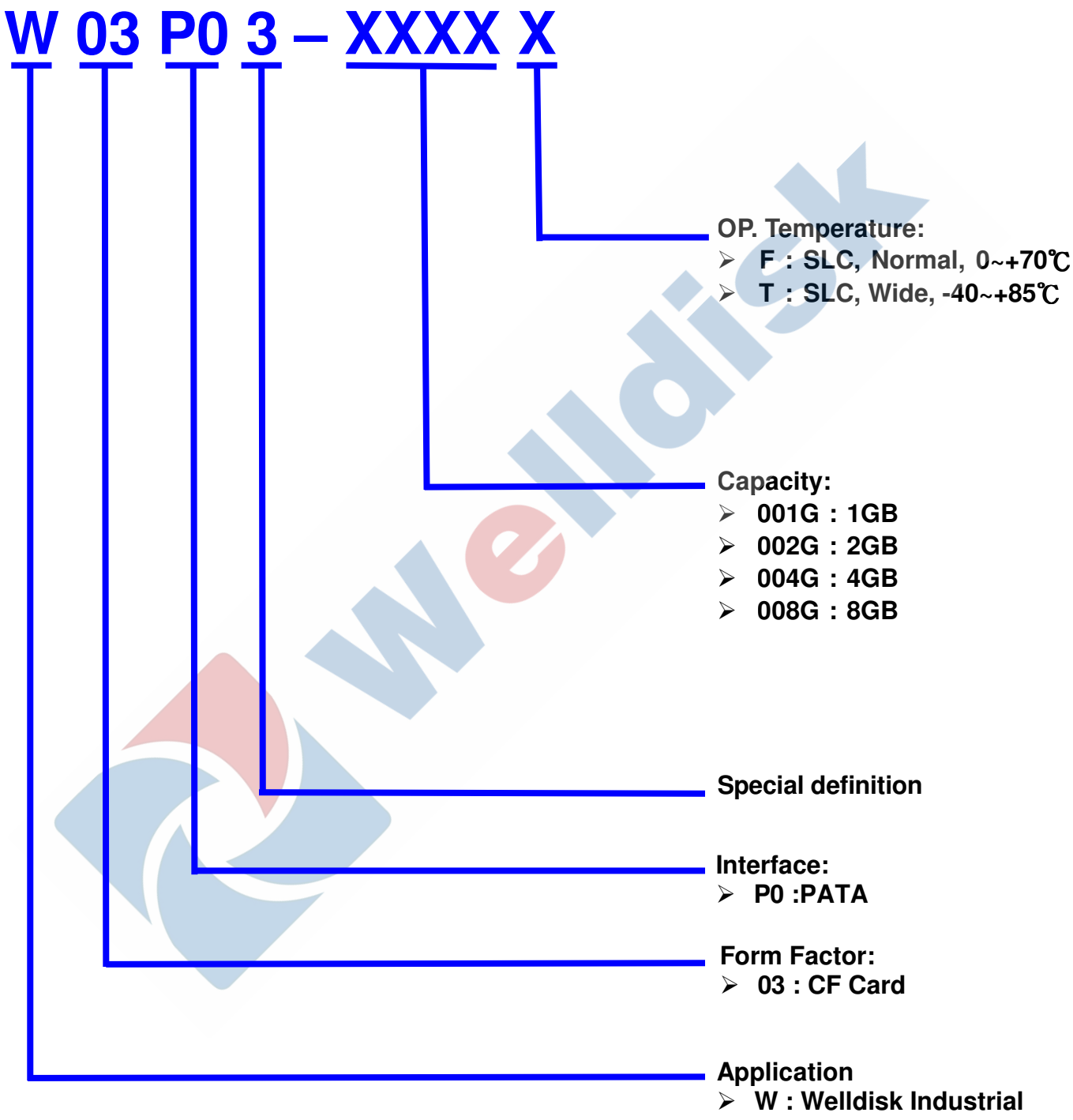
-REG (PC Card Memory Mode – Except Ultra DMA Protocol Active) Attribute Memory Select -REG (PC Card I/O Mode – Except Ultra DMA Protocol Active) -DMACK (PC Card Memory Mode when Ultra DMA Protocol Active) DMACK (PC Card I/O Mode when Ultra DMA Protocol Active) -DMACK (True IDE Mode)	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. In PC Card Memory Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal negated during the execution of any DMA Command by the device. The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus. In PC Card I/O Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal asserted during the execution of any DMA Command by the device. This is a DMA Acknowledge signal that is asserted by the host in response to (-) DMARQ to initiate DMA transfers. In True IDE Mode, while DMA operations are not active, the card shall ignore the (-) DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both
RESET (PC Card Memory Mode)	I	41	The CompactFlash Storage Card or CF+ Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode) -RESET (True IDE Mode)			This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode, this input pin is the active low hardware reset from the host.

VCC (PC Card Memory Mode) VCC (PC Card I/O Mode) VCC (True IDE Mode)	--	13,38	+5 V, +3.3 V power. This signal is the same for all modes. This signal is the same for all modes.
-VS1 -VS2 (PC Card Memory Mode) -VS1 -VS2 (PC Card I/O Mode) -VS1 -VS2 (True IDE Mode)	O	33 40	Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host so that the CompactFlash Storage Card or CF+ Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card. This signal is the same for all modes. This signal is the same for all modes.
-WAIT (PC Card Memory Mode – Except Ultra DMA Protocol Active) -WAIT (PC Card I/O Mode – Except Ultra DMA Protocol Active) IORDY (True IDE Mode – Except Ultra DMA Protocol Active) -DDMARDY (All Modes – Ultra DMA Write Protocol Active) DSTROBE (All Modes – Ultra DMA Read Protocol Active)	O	42	The -WAIT signal is driven low by the CompactFlash Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY. In all modes, when Ultra DMA mode DMA Write is active, this signal is asserted by the device during a data burst to indicate that the device is ready to receive Ultra DMA data out bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer. In all modes, when Ultra DMA mode DMA Read is active, this signal is the data in strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data in burst.

-WE (PC Card Memory Mode) -WE (PC Card I/O Mode) -WE (True IDE Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers. In PC Card I/O Mode, this signal is used for writing the configuration registers. In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode) Write Protect -IOIS16 (PC Card I/O Mode) -IOCS16 (True IDE Mode)	O	24	Memory Mode – The CompactFlash Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. I/O Operation – When the CompactFlash Storage Card or CF+ Card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port. In True IDE Mode, this output signal is asserted low when this device is expecting a word data transfer cycle.

5.PHYSICAL DIMENSION

Dimension: 36.4mm (L) x 42.8mm (W) x 3.3mm (H)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