Welldisk Technology Corp.

SATA 6Gb/s mSATA SSD Datasheet

W30S31

MLC : 16GB, 32GB, 64GB, 128GB, 256GB,512GB,1TB

SLC: 4GB, 8GB, 16GB, 32GB, 64GB, 128GB

Version 2.0

Document Number: RAP-000842

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Key Features:

- **Capacity:**
  - MLC : 16GB, 32GB, 64GB, 128GB, 256GB,512GB,1TB
  - SLC : 4GB, 8GB, 16GB, 32GB, 64GB, 128GB
- **Form Factor:** mSATA
- **Compatibility:**
  - Serial ATA 6Gb/s interface
  - Complies with ATA-8 Standard
  - Complies ATA Revision 3.1
  - S.M.A.R.T feature supported
  - NCQ Command set supported
  - PLP Function (Option)
- **Performance**
  - Sequential Read: Up to 561MB/s
  - Sequential Write: Up to 451MB/s
  - Random 4K Read: Up to 71K
  - Random 4K Write: Up to 79K
- **Power Consumption:**
  - Slumber : 0.02W- Typical
  - Idle : 0.04W-Typical
  - Sequential Read : 1.6W-Typical
  - Sequential Write : 3W-Typical
- **Temperature:**
  - Operation: -10°C ~ 80°C(Normal)
  - Operation: -40°C ~ 90°C(Wide)
  - Non-operation: -55°C ~ 95°C
- **Shock**
  - 1500G/0.5ms
- **Vibration**
  - 20G Peak, 10~2000Hz
- **Reliability**
  - MTBF: 1,500,000 hours
- **Function**
  - PLP (Option)

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Revision History

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0	Draft Version	Jun.2016		Terry_Chu
1	Add 16GB	July,2017		Terry_Chu

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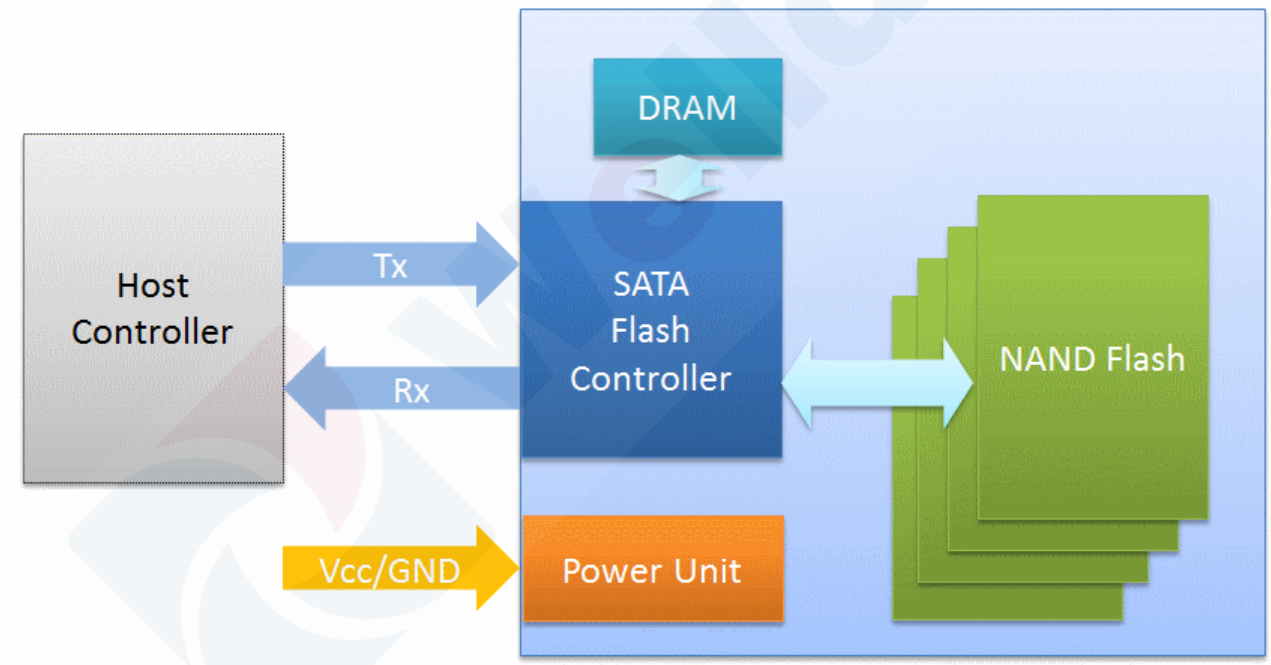
Table of Contents

2.0 Mechanical Specification 6
2.1 Physical dimensions and Weight 6
2.2 PCBA Dimensions 6
3.0 Product Specification 7
3.1 Interface and configuration 7
3.2 Capacity 7
3.3 Performance 8
3.3.1 Read/Write & IOPS Performance 8
3.4 Electrical 10
3.4.1 Operating Voltage 10
3.4.2 Power Consumption (Typical) 10
3.5 Environmental Conditions 11
3.6 Reliability 12
3.7 Endurance 12
3.8 PLP (Power Loss Protection) Option 12
4.0 Supported Command Sets 15
4.1 ATA Feature Command Sets 15
4.2 Identify Device 17
4.2.1 Identify device information 17
4.3 S.M.A.R.T. Feature Set 20
4.3.1 SMART Data Structure 21
4.3.2 SMART Attribute 22
5.0 Pin assignment and descriptions 24
5.1 SATA Interface 24
6.0 SATA Interface 27
6.1 Out of bank signaling 27
6.2 COMRESET sequence state diagram 28
6.3 COMINIT 30
6.4 Power on sequence timing diagram 31
7.0 Order Information 34
7.1 Model Number 34
8.0 Label & Package Specifications 35

1.0 General Description

Taking the advantages of NAND flash memory, Solid State Drive (SSD) provides better solutions on durability, performance, and power efficiency over traditional hard disk drives. Employing static wear-leveling technology to maximize SSD lifetime, the SSD solutions are your best choice on wide-ranged mobile computing devices and industrial electronic products. With standard SATA form factor or customized module form factor, The Welldisk mSATA SSD ISS332 offers capacities up to 512GB using Synchronous MLC NAND type flash memories.



[**Figure 1-1**] **Functional Block Diagram**

2.0 Mechanical Specification

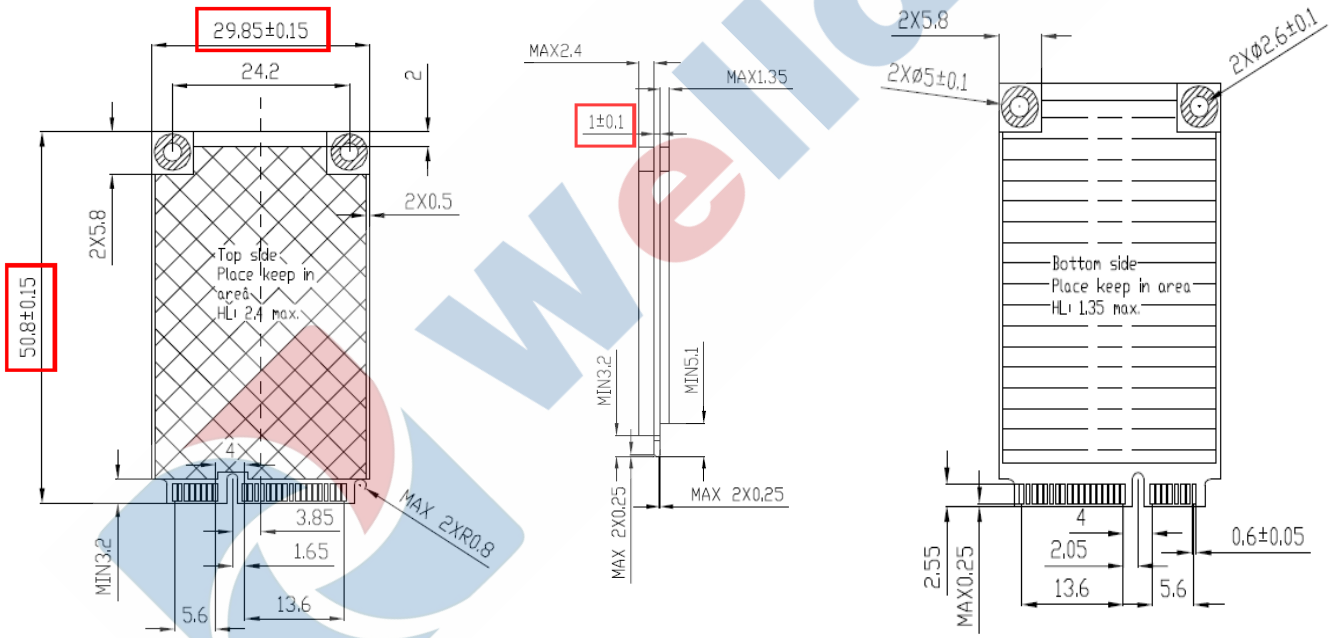
"All product specifications not covered in this document (electrical performance, appearance, etc.) are in accordance with Welldisk's defined norms and standards. "

2.1 Physical dimensions and Weight

[Table 2-1] Dimensions and Weight

Length(mm)	Width(mm)	Height(mm)	Weight(gram)
50.80+0.15/-0.18	29.85+/-0.15	Max 3.85	Max 5

2.2 PCBA Dimensions



[Figure 2-1] Physical Dimensions

3.0 Product Specification

3.1 Interface and configuration

- Burst read/write rate is 600 MB/sec (6.0 Gb/sec).
- Supports 1-port 1.5/3.0/6.0 Gbps SATA I/II/III interface.
- Compliant with Serial ATA International Organization: Serial ATA Revision 3.1.
- Compliant SSD Alliance compliance program

3.2 Capacity

Model		IMMS332		
Capacity	Cylinder	Head	Sector	Total Sectors
16GB	16383	16	63	31,277,232
32GB	16383	16	63	62,533,296
64GB	16383	16	63	125,045,424
128GB	16383	16	63	250,069,680
256GB	16383	16	63	500,118,192
512GB	16383	16	63	1,000,215,216
1TB	16383	16	63	2,000,409,264

[**Table 3-1**] **User Addressable Sectors**

Total useable capacity may be less (duo to formatting, flash management, and other functions).

1GB=1,000,000,000 bytes; 1sector = 512bytes.

3.3 Performance

3.3.1 Read/Write & IOPS Performance

MLC	16GB	32GB	64GB	128GB	256GB	512GB	1TB	Unit
4K Random Read	13K	26K	50K	70K	71K	70K	70K	IOPS
4K Random Write	5K	11K	24K	46K	79K	73K	73K	IOPS

SLC	4GB	8GB	16GB	32GB	64GB	128GB	Unit
4K Random Read	16K	32K	60K	76K	77K	76K	IOPS
4K Random Write	7.6K	15K	30K	58K	74K	73K	IOPS

[Table 3-2] Read/Write & IOPS Performance

- IOPS Test Utility: IOmeter 2010 (Queue depth of 32; Measurements are performed on 10% capacity of LBA range. Write cache enable)
- The system conditions and test environment may affect test result

MLC	16GB	32GB	64GB	128GB	256GB	512GB	1TB	Unit
Sequential Read	140	277	512	520	509	523	523	MB/s
Sequential Write	24	48	97	191	373	448	448	MB/s

SLC	4GB	8GB	16GB	32GB	64GB	128GB	Unit
Sequential Read	120	240	460	510	520	520	MB/s
Sequential Write	33	67	130	260	380	420	MB/s

[Table 3-3] Read/Write Performance (Crystal Disk Mark)

- Seq. Read & Write speed test by Crystal Disk Mark
- The system conditions and test environment may affect test result

MLC	16GB	32GB	64GB	128GB	256GB	512GB	1TB	Unit
Sequential Read	140	281	550	560	560	560	560	MB/s
Sequential Write	24	49	97	192	375	451	420	MB/s

SLC	4GB	8GB	16GB	32GB	64GB	128GB	Unit
Sequential Read	125	240	490	560	560	560	MB/s
Sequential Write	33	67	130	260	390	430	MB/s

[Table 3-4] Read/Write Performance (ATTO)

- Seq. Read & Write speed test by ATTO
- The system conditions and test environment may affect test result

3.4 Electrical

3.4.1 Operating Voltage

Operating Voltage	
Input Power	DC 3.3V ± 5%
Maximum Ripple	100Mv p-p or less

[Table 3-5] Operating Voltage

3.4.2 Power Consumption (Typical)

MLC	Slumber	Partial	Idle	Read	Write	Unit
16GB	0.03	0.08	0.28	0.95	0.88	W
32GB	0.03	0.08	0.28	0.95	0.88	
64GB	0.03	0.07	0.28	1.09	1.45	
128GB	0.03	0.09	0.27	1.34	1.6	
256GB	0.04	0.17	0.32	1.45	2.55	
512GB	0.04	0.17	0.32	1.6	3.00	
1TB	0.07	0.12	0.4	2.0	4.6	
SLC	Slumber	Partial	Idle	Read	Write	
4GB	0.05	0.12	0.35	0.8	0.8	
8GB	0.05	0.12	0.35	1.1	1.1	
16GB	0.05	0.12	0.35	1.3	1.3	
32GB	0.05	0.12	0.35	1.6	1.8	
64GB	0.05	0.12	0.35	1.7	2.5	
128GB	0.05	0.12	0.35	1.7	2.6	

[Table 3-6] Power Consumption

- To measure consumption in /Slumber/ Idle mode and Sequential Read/Sequential Write

3.5 Environmental Conditions

Feature	Operating	Non-Operating
Normal Temperature	-10°C to 80°C	-55°C to 95°C
Wide Temperature	-40°C to 90°C	-55°C to 95°C
Humidity	0℃ to 55℃ / 5%~95% RH, non-condensing	
Vibration	20G Peak, 10~2000Hz	
Shock	1500G, duration 0.5ms, Half Sine Wave	

[Table 3-7] Temperature, Humidity, Shock, Vibration

3.6 Reliability

Parameter	Value
Mean Time Between Failures (MTBF) The MTBF statistics were calculated by Part Count Method, not relevant to individual units	1,500,000 hours

[Table 3-8] Reliability Specification

3.7 Endurance

Endurance for the SSD can be predicted based on the operating workload .The tables as below shows the drive lifetime for each SSD capacity based JESD219A Client workload.

MLC	16GB	32GB	64GB	128GB	256GB	512GB	1TB	Unit
TBW	21	43	86	172	345	690	1381	TB

SLC	4GB	8GB	16GB	32GB	64GB	128GB	Unit
TBW	111	222	445	890	1781	3562	TB

[Table 3-9] Tera Byte Written

3.8 PLP (Power Loss Protection) Option

During a normal system shutdown, the operating system would issue STANDBY IMMEDIATE or FLUSH CACHE command to signal SSD drive to flush all system and user data in cache to NAND Flash to prepare for system shutdown, therefore preserving the data after the power is shutoff.

However, during an unintentional shutdown, the data in cache may not be able to be flushed to NAND Flash in time before power disappeared. It is very important for SSD drive to implement intelligent protection schemes to preserve data integrity in the case of unexpected power loss. An intelligent hardware architecture showing in the following picture, is to combine sensitive voltage monitors with banks of power-retaining capacitors. Welldisk's PLP supplies its SSDs with enough power to continue buffered read-write

operations until completion. When a power loss occurs, the power monitor circuit detects the power drop and instructs the controller to back up all data in the buffer before the power drains from the capacitor banks. Using this method, all important data is saved without corruption.

By implementing PLP function including HW and FW, voltage detection circuit will detect the voltage drop and deliver the alarm to SSD FW. This process guarantees the integrity of all data and also gets rid of the risk of data and FW lost.

Figure 5-1 PLP architecture

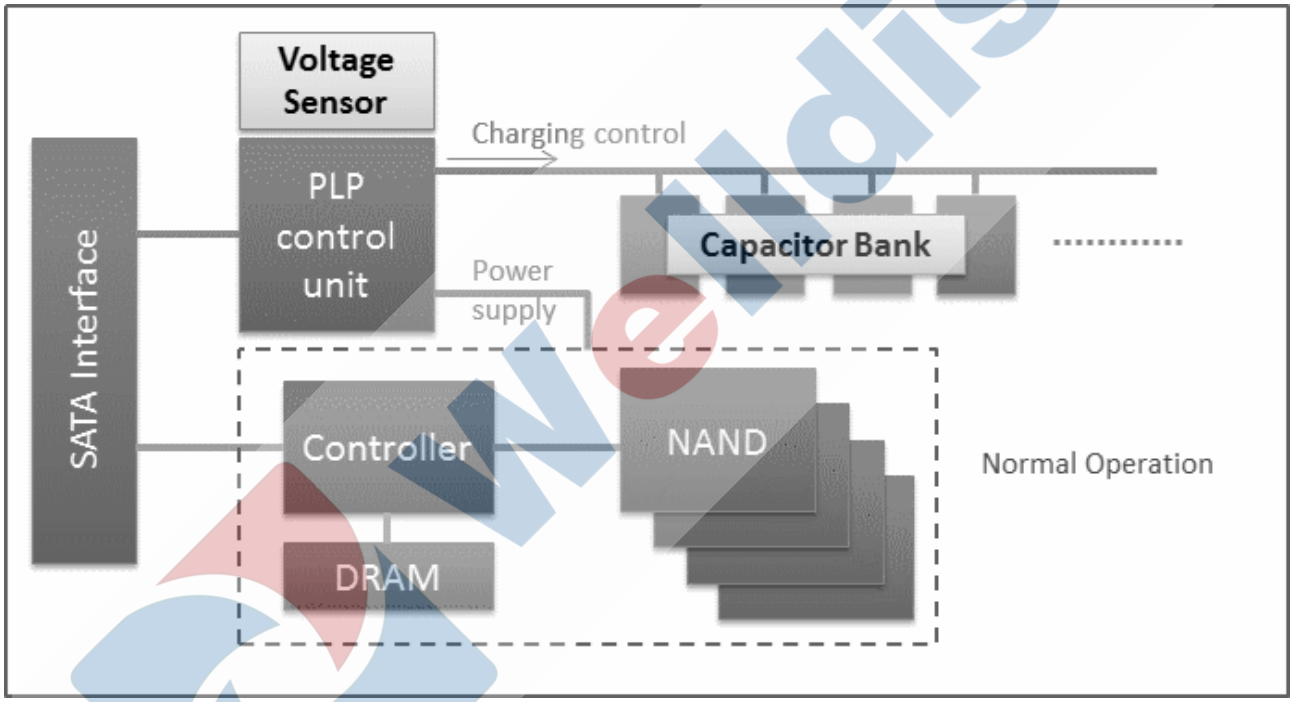
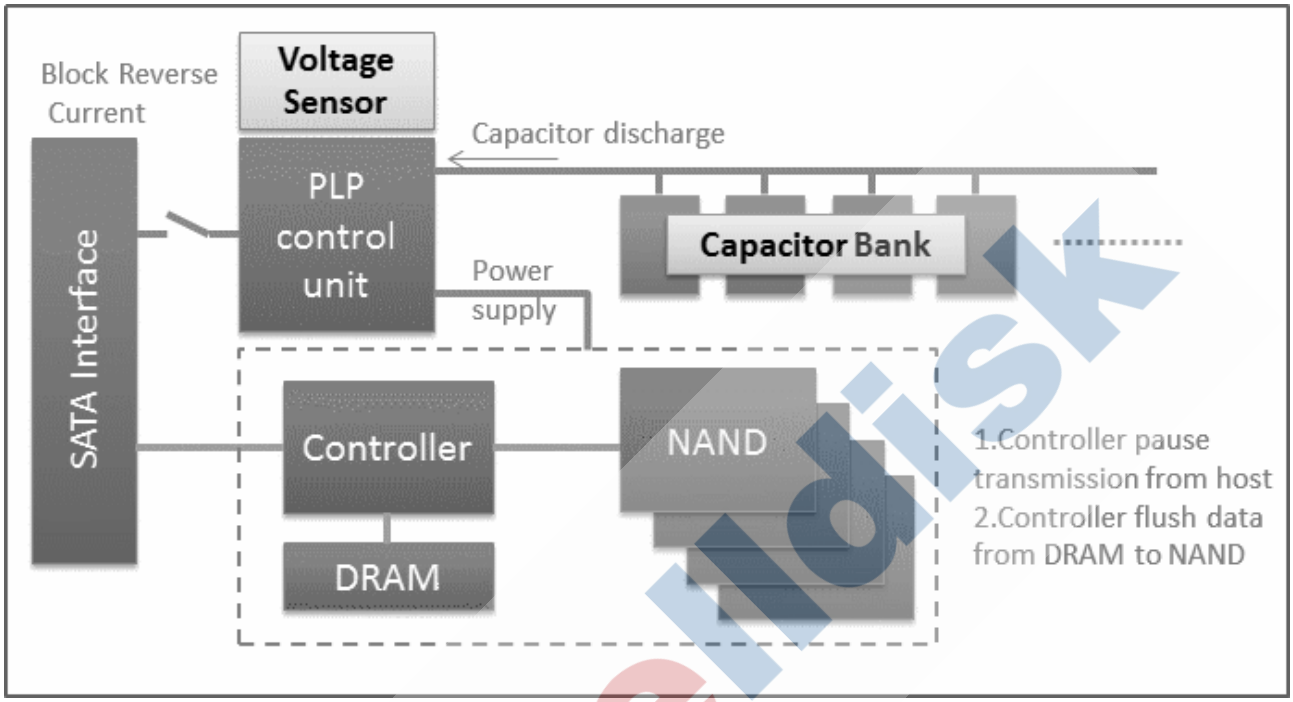


Figure 5-2 PLP Operation



4.0 Supported Command Sets

4.1 ATA Feature Command Sets

Welldisk W30S31 supports all the mandatory ATA commands defined in ATA-8 specification. The supported command sets are listed as below.

[Table 4-1] Supported ATA Command Table

Command Name	Code	Protocol
General Feature Set		
Execute Device Diagnostic	90h	Execute device diagnostic
Flush Cache	E7h	Non-data
Identify Device	ECh	PIO data-in
Initialize Drive Parameters	91h	Non-data
Read DMA	C8h	DMA
Read Log Ext	2Fh	PIO data-in
Read Multiple	C4h	PIO data-in
Read Sector(s)	20h	PIO data-in
Read Verify Sector(s)	40h or 41h	Non-data
Set Feature	EFh	Non-data
Set Multiple Mode	C6h	Non-data
Write DMA	CAh	DMA
Write Multiple	C5h	PIO data-out
Write Sector(s)	30h	PIO data-out
NOP	00h	Non-data
Read Buffer	E4h	PIO data-in
Write Buffer	E8h	PIO data-out
Power Management Feature Set		
Check Power Mode	E5h or 98h	Non-data
Idle	E3h or 97h	Non-data
Idle Immediate	E1h or 95h	Non-data
Sleep	E6h or 99h	Non-data
Standby	E2h or 96h	Non-data

Standby Immediate	E0h or 94h	Non-data
Security Mode Feature Set		
Security Set Password	F1h	PIO data-out
Security Unlock	F2h	PIO data-out
Security Erase Prepare	F3h	Non-data
Security Erase Unit	F4h	PIO data-out
Security Freeze Lock	F5h	Non-data
Security Disable Password	F6h	PIO data-out
SMART Feature Set		
SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Execute OFF-LINE Immediate	B0h	Non-data
SMART Read Log	B0h	PIO data-in
SMART Read Data	B0h	PIO data-in
SMART Read Threshold	B0h	PIO data-in
SMART Return Status	B0h	Non-data
SMART Save Attribute Values	B0h	Non-data
SMART Write Log	B0h	PIO data-out
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
48-bit Address Feature Set		
Flush Cache Ext	EAh	Non-data
Read Sector(s) Ext	24h	PIO data-in
Read DMA Ext	25h	DMA
Read Multiple Ext	29h	PIO data-in
Read Native Max Address Ext	27h	Non-data

Read Verify Sector(s) Ext	42h	Non-data
Set Max Address Ext	37h	Non-data
Write DMA Ext	35h	DMA
Write Multiple Ext	39h	PIO data-out
Write Sector(s) Ext	34h	PIO data-out
NCQ Feature Set		
Read FPDMA Queued	60h	DMA Queued
Write FPDMA Queued	61h	DMA Queued
Others		
Data Set Management	06h	DMA
Seek	70h	Non-data

4.2 Identify Device

Welldisk W30S31 responds to ATA IDENTIFY DEVICE command with a pre-defined

string of information on features, hardware and firmware revision information.

4.2.1 Identify device information

[**Table 4-2**] **IDENTIFY DEVICE Table**

Word	F / V	Default Value	Description
0	F	044Ah	General configuration
1	X	XXXXh	Default number of cylinders
2	V	0000h	Reserved
3	X	00XXh	Default number of heads
4	X	0000h	Obsolete
5	X	0240h	Obsolete
6	F	XXXXh	Default number of sectors per track
7 - 8	V	XXXXh	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	X	0000h	Obsolete
10 - 19	F	XXXXh	Serial number in ASCII (Right justified)
20	X	0002h	Obsolete

21	X	0002h	Obsolete
22	X	0000h	Obsolete
23 - 26	F	XXXXh	Firmware revision in ASCII Big Endian Byte Order in Word
27 - 46	F	XXXXh	Model number in ASCII (Left justified) Big Endian Byte Order in Word
47	F	8001h	Maximum number of sectors on Read/Write Multiple command
48	F	0000h	Reserved
49	F	0300h	Capabilities
50	F	0400h	Capabilities
51	F	0200h	PIO data transfer cycle timing mode
52	X	0000h	Obsolete
53	F	0007h	Field validity
54	X	XXXXh	Current numbers of cylinders
55	X	XXXXh	Current numbers of heads
56	X	XXXXh	Current sectors per track
57 - 58	X	XXXXh	Current capacity in sectors (LBAs) (Word 57 = LSW , Word 58 = MSW)
59	F	0101h	Multiple sector setting
60 - 61	F	XXXXh	Total number of user addressable logical sectors for 28-bit commands (DWord)
62	X	0000h	Reserved
63	F	0207h	Multiword DMA transfer Supports MDMA mode 0, 1 and 2
64	F	0003h	Advanced PIO modes supported
65	F	0078h	Minimum Multiword DMA transfer cycle time per word
66	F	0078h	Recommended Multiword DMA transfer cycle time
67	F	0078h	Minimum PIO transfer cycle time without flow control
68	F	0078h	Minimum PIO transfer cycle time with IORDY flow control
69	F	4000h	Additional supported

70 - 74	F	0000h	Reserved
75	F	001Fh	Queue depth
76	F	030Eh	Serial ATA capabilities • Supports Serial ATA Gen3 • Supports Serial ATA Gen2 • Supports Serial ATA Gen1 • Supports Phy event counters log • Supports receipt of host initiated power management requests • Supports Native Command Queuing
77	F	0080h	Serial ATA additional capability • DevSleep_to_ReducedPwerState
78	F	0148h	Serial ATA features supported • Supports Device Sleep • Supports software settings preservation • Device supports initiating power management
79	V	0040h	Reserved
80	F	03FCh	Major version number (ACS-2)
81	F	0000h	Minor version number
82	F	702Bh	Command sets supported 0
83	F	7500h	Command sets supported 1
84	F	4002h	Command sets supported 2
85 - 87	V	XXXXh	Command set/feature enabled
88	V	007Fh	Ultra DMA mode supported and selected
89	F	0003h	Time required for a Normal Erase mode Security Erase Unit command
90	F	0001h	Time required for an Enhanced Erase mode Security Erase Unit command
91	V	0000h	Current advanced power management value
92	V	FFFEh	Master password identifier
93 - 99	V	0000h	Reserved
100 - 103	V	XXXXh	Maximum user LBA for 48-bit address feature set

104	V	0000h	Reserved
105	F	0100h	Maximum number of 512-byte blocks per Data Set Management command
106 - 127	V	0000h	Reserved
128	V	0009h	Security status
129 - 159	X	XXXXh	Vendor specific
160	F	0000h	Power requirement description
161	X	0000h	Reserved
162	F	0000h	Key management schemes supported
163	F	0000h	CF Advanced True IDE Timing mode capability and setting
164 - 168	V	0000h	Reserved
169	F	0001h	Data Set Management supported
170 - 216	V	XXXXh	Reserved
217	F	0001h	Non-rotating media (SSD)
218 - 221	X	0000h	Reserved
222	F	107Fh	Transport major revision (SATA Rev 3.1)
223 - 254	X	0000h	Reserved
255	X	XXXXh	Integrity word

Notes:

1. F = content (byte) is fixed and does not change.

2. V = content (byte) is variable and may change depending on the state of the device or the commands executed by the device.

3. X = content (byte) is vendor specific and may be fixed or variable.

4.3 S.M.A.R.T. Feature Set

S.M.A.R.T. (Self-Monitoring, Analysis and Reporting Technology; often written as SMART) is a monitoring system for HDDs and SSDs to detect and report on various indicators of reliability and drive status. Host can monitor the healthy condition of SSD drive by analyzing S.M.A.R.T. data and inform user to take action if necessary. W30S31 supports specific S.M.A.R.T. for industrial and server application including drive life monitoring, wear leveling, total data read/write on host/flash interface. By leveraging S.M.A.R.T., user can easily not only monitor drive status but also understand the workload to help evaluating the reliability.

[Table 4-3] S.M.A.R.T. Feature Register Values

Value	Command	Value	Command
D0h	Read Data	D5h	Read Log
D1h	Read Attribute Threshold	D6h	Write Log
D2h	Enable/Disable Autosave	D8h	Enable SMART operations
D3h	Save Attribute Values	D9h	Disable SMART operations
D4h	Execute Off-Line Immediate	DAh	Return Status

If the reserved size is below the threshold, the status can be read from the Cylinder Register using **Return Status** command (DAh).

4.3.1 SMART Data Structure

The following 512byte make up the device SMART data structure. Users can obtain the data using **Read Data** command (D0h).

[Table 4-4] S.M.A.R.T. Data Structure

Byte	F / V	Description
0 – 1	X	Revision code
2 – 361	X	SMART attribute & value [Table 4-3.3]
362	V	Off-line data collection status
363	X	Self-test execution status byte
364 – 365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368 – 369	F	SMART capability
370	F	Error logging capability Bit 7-1 : Reserved Bit 0 = 1 : Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375 – 385	R	Reserved
386 – 395	F	Firmware version
396 – 399	F	Reserved

Byte	F / V	Description
400 – 405	F	“SM2246”
406 – 510	X	Vendor specific
511	V	Data structure checksum

Notes:

F = content (byte) is fixed and does not change.

V = content (byte) is variable and may change depending on the state of the device or commands executed by the device.

X = content (byte) is vendor specific and may be fixed or variable.

R = content (byte) is reserved and shall be zero.

4.3.2 SMART Attribute

The following table defines the vendor specific data in byte 2 to 361 of the 512-byte SMART data.

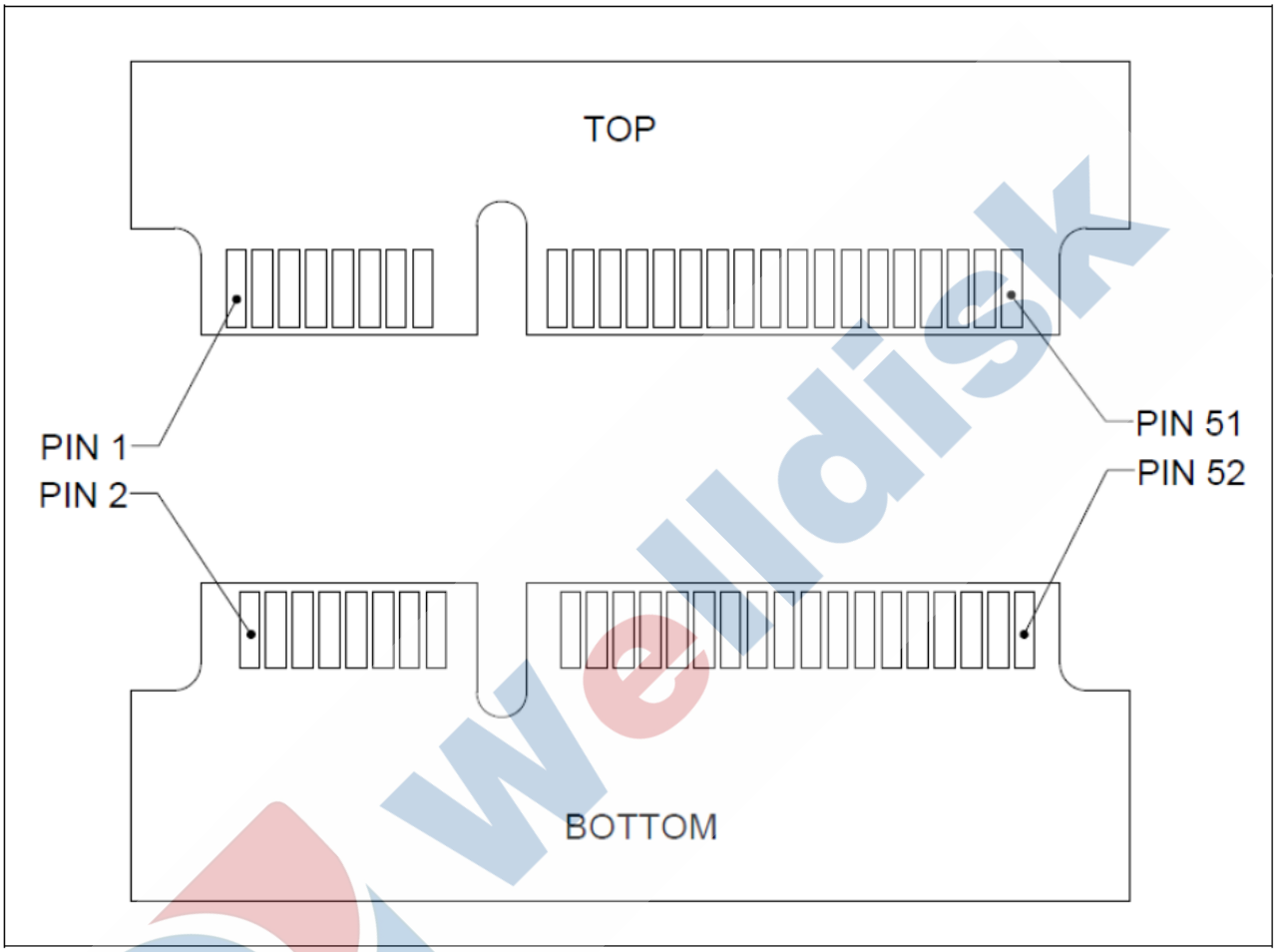
[Table 4-3.3]S.M.A.R.T. Atribute

Attribute ID (hex)	Raw Attribute Value						Attribute Name
01	MSB	00	00	00	00	00	Read error rate
05	LSB	MSB	00	00	00	00	Reallocated sectors count
09	LSB	-	-	MSB	00	00	Reserved
0C	LSB	-	-	MSB	00	00	Power cycle count
A0	LSB	-	-	MSB	00	00	Uncorrectable sector count when read/write
A1	LSB	MSB	00	00	00	00	Number of valid spare block
A3	LSB	MSB	00	00	00	00	Number of initial invalid block
A4	LSB	-	-	MSB	00	00	Total erase count
A5	LSB	-	-	MSB	00	00	Maximum erase count
A6	LSB	-	-	MSB	00	00	Minimum erase count
A7	LSB	-	-	MSB	00	00	Average erase count
A8	LSB	-	-	MSB	00	00	Max. erase count of Spec.
A9	LSB	-	-	MSB	00	00	Remain Life(percentage)
AF	LSB	-	-	MSB	00	00	Program fail count in worst die
B0	LSB	MSB	00	00	00	00	Erase fail count in worst die
B1	LSB	-	-	MSB	00	00	Total wear level count
B2	LSB	MSB	00	00	00	00	Runtime invalid block count
B5	LSB	-	-	MSB	00	00	Total program fail count

Attribute ID (hex)	Raw Attribute Value						Attribute Name
B6	LSB	MSB	00	00	00	00	Total erase fail count
C0	LSB	MSB	00	00	00	00	Power-off retract count
C2	MSB	00	00	00	00	00	Controlled temperature
C3	LSB	-	-	MSB	00	00	Hardware ECC recovered
C4	LSB	-	-	MSB	00	00	Reallocation event count
C5	LSB	-	-	MSB	00	00	Current pending sector count
C6	LSB	-	-	MSB	00	00	Uncorrectable error count off-line
C7	LSB	MSB	00	00	00	00	Ultra DMA CRC error count
E8	LSB	MSB	00	00	00	00	Available reserved space
F1	LSB	-	-	-	-	MSB	Host written LBAs (each write unit = 32MB)
F2	LSB	-	-	-	-	MSB	Host read LBAs (each read unit = 32MB)
F5	LSB	-	-	-	-	MSB	Total data written to flash (each write unit = 32MB)

5.0 Pin assignment and descriptions

5.1 SATA Interface



[Figure 5-1] SATA Interface

Pins	P1	Reserved	No Connect
	P2	+3.3V	3.3V Source
	P3	Reserved	No Connect
	P4	GND	Ground
	P5	Reserved	No Connect
	P6	+1.5V	No Connect
	P7	Reserved	No Connect
	P8	Reserved	No Connect
	P9	GND	Ground

	P10	Reserved	No Connect
	P11	Reserved	No Connect
	P12	Reserved	No Connect
	P13	Reserved	No Connect
	P14	Reserved	No Connect
	P15	GND	Ground
	P16	Reserved	No Connect
	P17	Reserved	No Connect
	P18	GND	Ground
	P19	Reserved	No Connect
	P20	Reserved	No Connect
	P21	GND	Ground
	P22	Reserved	No Connect
	P23	+B	Host Receiver Differential Signal Pair (This is an output of the SSD)
	P24	+3.3V	3.3V Source
	P25	-B	Host Receiver Differential Signal Pair (This is an output of the SSD)
	P26	GND	Ground
	P27	GND	Ground
	P28	+1.5V	No Connect
	P29	GND	Ground
	P30	Two wire Interface	No Connect
	P31	-A	Host Transmitter Differential Signal Pair (This is an input of the SSD)
	P32	Two wire Interface	No Connect
	P33	+A	Host Transmitter Differential Signal Pair (This is an input of the SSD)
	P34	GND	Ground
	P35	GND	Ground
	P36	Reserved	No Connect
	P37	GND	Ground
	P38	Reserved	No Connect
	P39	+3.3V	3.3V Source
	P40	GND	Ground
	P41	+3.3V	3.3V Source

	P42	Reserved	No Connect
	P43	Device Type	No Connect
	P44	DevSleep	Device Sleep pin
	P45	Vendor	No Connect
	P46	Reserved	No Connect
	P47	Vendor	No Connect
	P48	+1.5V	No Connect
	P49	DAS/DSS	Device Activity Signal
	P50	GND	Ground
	P51	Presence Detection	Ground
	P52	+3.3V	3.3V Source

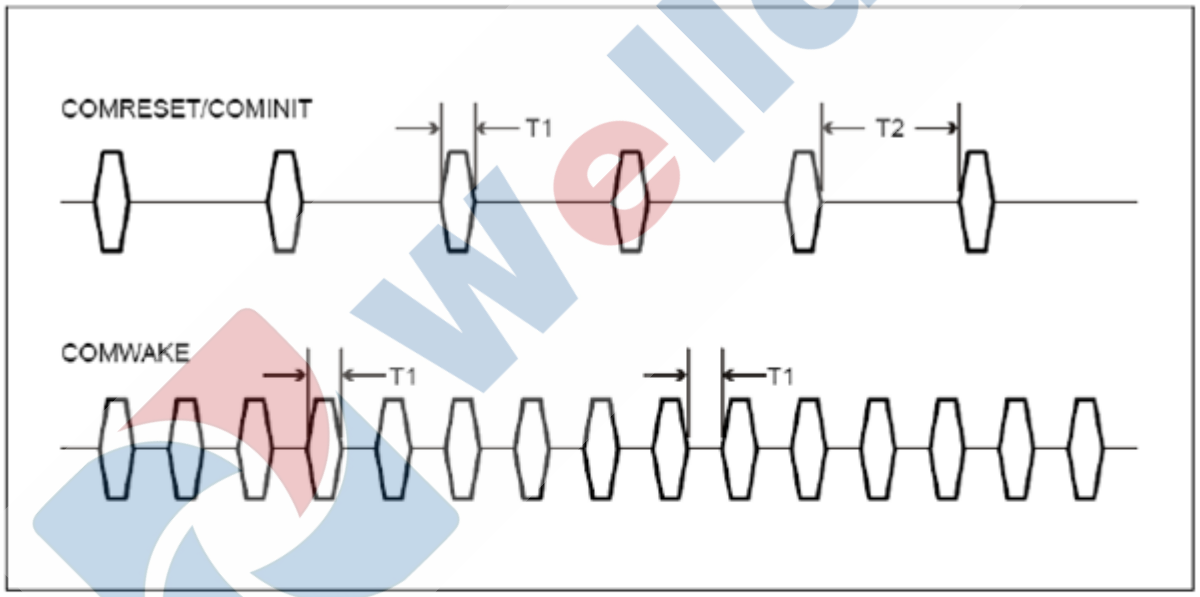
[Table 5-2] SATA Pin Assignment

6.0 SATA Interface

6.1 Out of bank signaling

The shall be tree Out Of Band (OOB) signals used/ detected by the Phy: COMRESET, COMINIT, and COMWAKE. Each burst is followed by idle periods (at common-mode levels), having durations as depicted in following Figure and Table. The COMWAKE OOB signaling is used to bring the Phy out of a power-down state (Partial or Slumber).

There shall be three Out Of Band (OOB) signals used/detected by the Phy: COMRESET, COMINIT, and COMWAKE. COMINIT, COMRESET and COMWAKE OOB signaling shall be achieved by transmission of either a burst of four Gen1 ALIGNP primitives or a burst composed of four Gen1 Dwords with each Dword composed of four D24.3 characters, each burst having duration of 160 UIOOB. Each burst is followed by idle periods (at common-mode levels), having durations as depicted in Figure 6-1 and Table 6-1.



[Figure 6-1] OOB signals

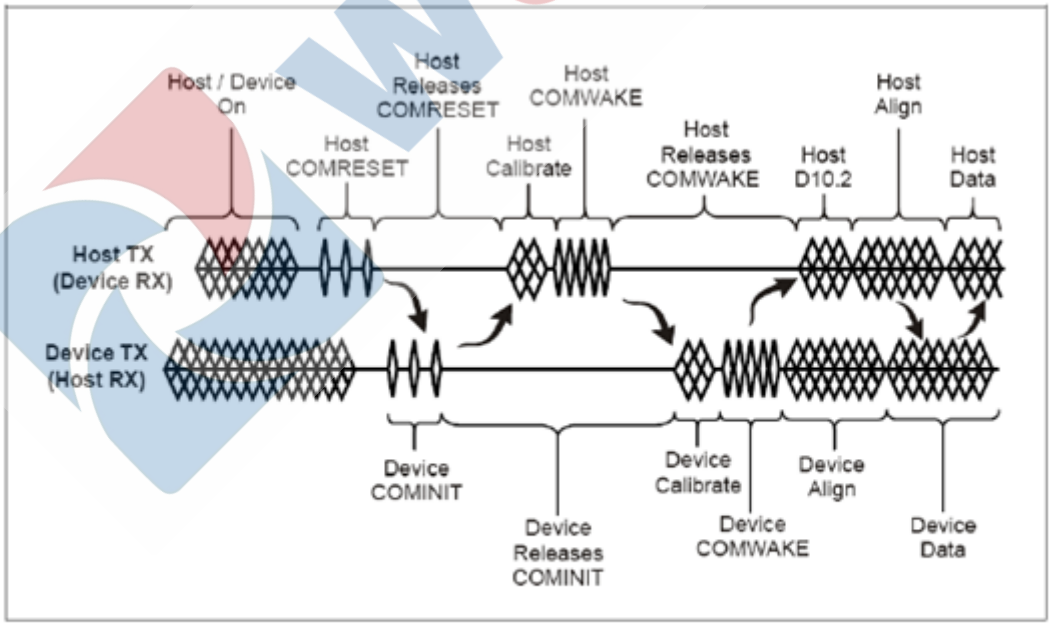
Time	Value
T1	160 Uloob (106.7 ns nominal)
T2	480 Uloob (320 ns nominal)

[Table 6-1] OOB Signal Times

6.2 COMRESET sequence state diagram

COMRESET always originates from the host controller, and forces a hardware reset in the device. It is indicated by transmitting bursts of data separated by an idle bus condition. The OOB COMRESET signal shall consist of no less than six data bursts, including inter-burst temporal spacing. The COMRESET signal shall be:
1) Sustained/continued uninterrupted as long as the system hard reset is asserted, or 2) Started during the system hardware reset and ended sometime after the negation of system hardware reset, or 3) Transmitted immediately following the negation of the system hardware reset signal.

The host controller shall ignore any signal received from the device from the assertion of the hardware reset signal until the COMRESET signal is transmitted. Each burst shall be 160 Gen1 UI's long (106.7 ns) and each inter-burst idle state shall be 480 Gen1 UI's long (320 ns). A COMRESET detector looks for four consecutive bursts with 320 ns spacing (nominal). Any spacing less than 175 ns or greater than 525 ns shall invalidate the COMRESET detector output. The COMRESET interface signal to the PHY layer shall initiate the Reset sequence shown in Figure 6-2 below. The interface shall be held inactive for at least 525 ns after the last burst to ensure far-end detector detects the negation properly.



[Figure 6-2] COMRESET Sequence

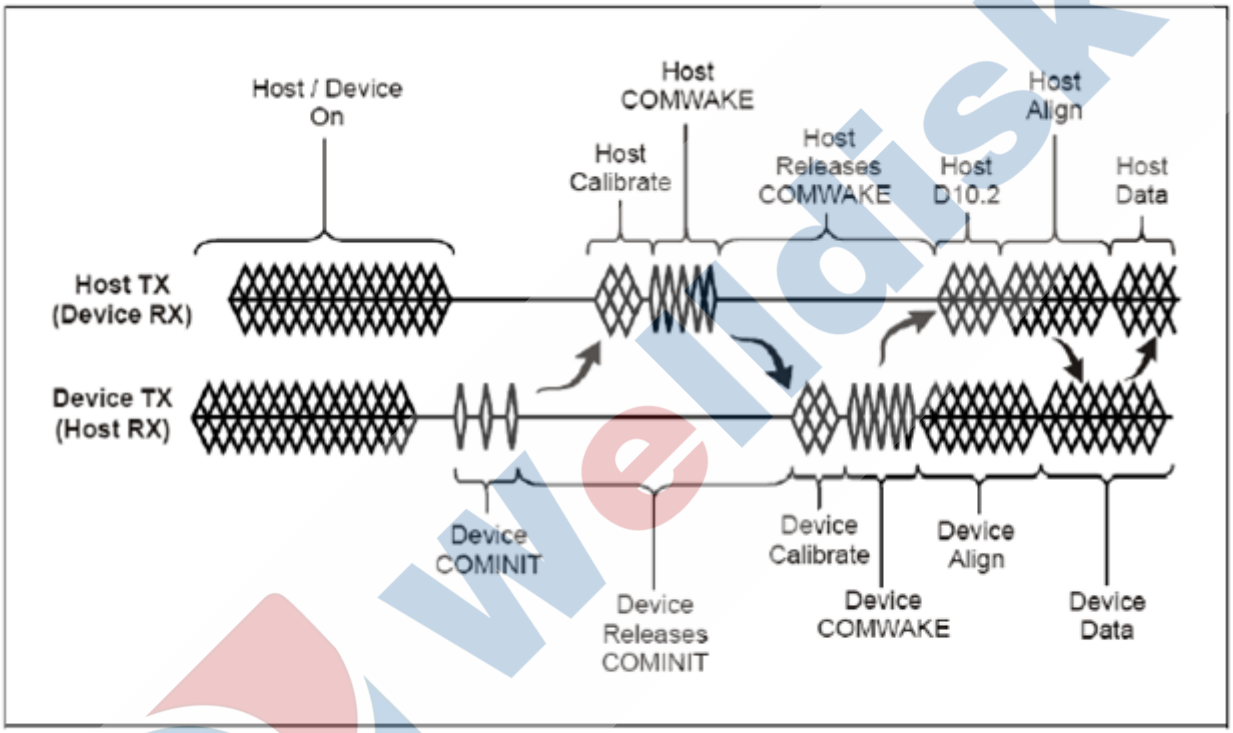
Description:

1. Host/device is powered and operating normally with some form of active communication.
2. Some condition in the host causes the host to issue COMRESET.
3. Host releases COMRESET. Once the condition causing the COMRESET is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.
4. Device issues COMINIT –When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.
5. Host calibrates and issues a COMWAKE.
6. Device responds –The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP Dwords have been sent for 54.6us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error state.
7. Host locks –after detecting the COMWAKE, the host starts transmitting D10.2 characters (see 7.6) at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This ensures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence –repeating indefinitely until told to stop by the Application layer.
8. Device locks –the device locks to the ALIGN sequence and, when ready, sends SYNCP indicating it is ready to start normal operation.

9. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

6.3 COMINIT

COMINIT always originates from the drive and requests a communication initialization. It is electrically identical to the COMRESET signal except that it originates from the device and is sent to the host. It is used by the device to request a reset from the host in accordance to the sequence shown in Figure 6-3, below.



[Figure 6-3] COMINIT Sequence

Description:

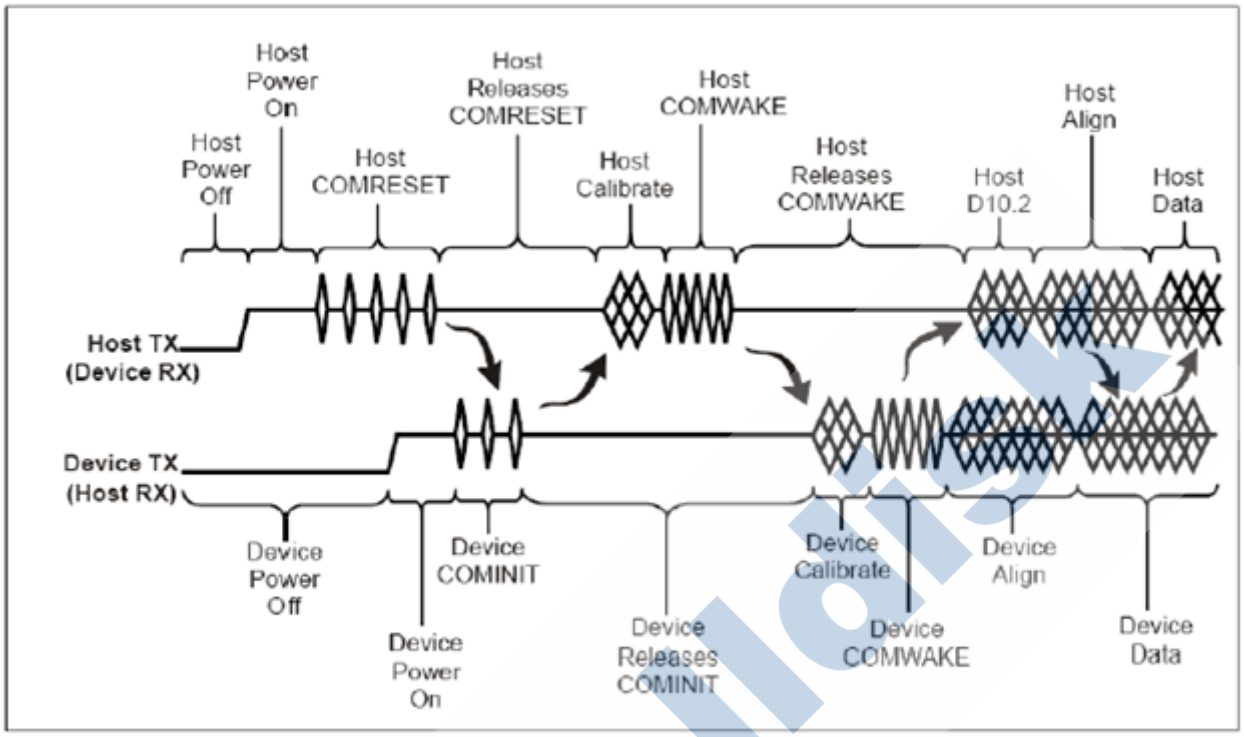
1. Host/device is powered and operating normally with some form of active communication.
2. Some condition in the device causes the device to issues a COMINIT
3. Host calibrates and issues a COMWAKE.
4. Device responds –The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP Dwords have been sent for 54.6 us (2048 nominal Gen1 Dword times) without a response from the host as determined by

detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error state.

5. Host locks –after detecting the COMWAKE, the host starts transmitting D10.2 characters (see section 7.6) at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6 us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This ensures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence –repeating indefinitely until told to stop by the Application layer.
6. Device locks –the device locks to the ALIGN sequence and, when ready, sends SYNCP indicating it is ready to start normal operation.
7. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

6.4 Power on sequence timing diagram

The following timing diagrams and descriptions are provided for clarity and are informative. The state diagrams provided in section 7.4 comprise the normative behavior specification and is the ultimate reference.



[Figure 6-4] Power on sequence

Description:

1. Host/device power-off -Host and device power-off.
2. Power is applied -Host side signal conditioning pulls TX and RX pairs to neutral state(common mode voltage).
3. Host issues COMRESET
4. Host releases COMRESET. Once the power-on reset is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.
5. Device issues COMINIT –When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.
6. Host calibrates and issues a COMWAKE.
7. Device responds –The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP primitives have been sent for 54.6 us (2048 nominal Gen1 Dword times) without a response from the host as

determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP primitives at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device shall enter an error state.

8. Host locks –after detecting the COMWAKE, the host starts transmitting D10.2characters (see 7.6) at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This insures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us(32768 nominal Gen1 Dword times) the host restarts the power-on sequence –repeating indefinitely until told to stop by the Application layer.
9. Device locks –the device locks to the ALIGN sequence and, when ready, sends the SYNCP primitive indicating it is ready to start normal operation.
10. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

7.0 Order Information

7.1 Model Number

W 30 S3 1– XXXX X X

Function :
- **P : PLP Function**

OP. Temperature:
- **M : MLC, Normal, -10~80˚C**

Capacity :
- **008G : 8GB 256G : 256GB**
- **016G : 16GB 512G : 512GB**
- **032G : 32GB 001T : 1TB**
- **064G : 64GB**
- **128G : 128GB**
- **128G : 128GB**

Special definition

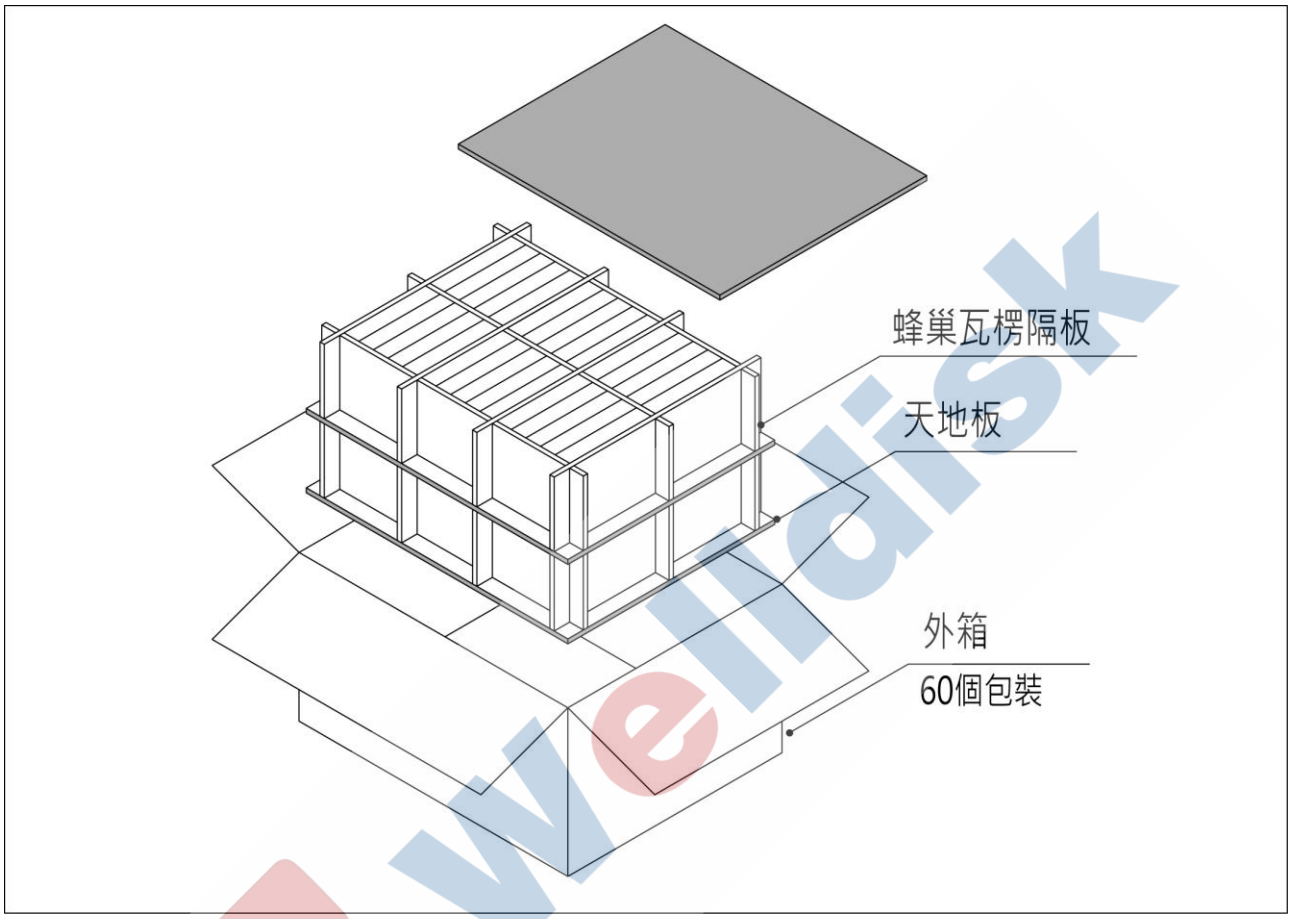
Interface:
- **S3 : SATA 3**

Form Factor:
- **30 :Msata**

Application:
- **W:Welldisk Industrial**

[Table 6-1] Product Line up

8.0 Label & Package Specifications



[Figure 8-1 Package